



**INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH  
TECHNOLOGY**

**INTRODUCTION OF VIRTUAL DC BUS IN A TRANSFORMERLESS GRID  
CONNECTED COST EFFECTIVE PV SYSTEM FOR THE ELIMINATION OF  
LEAKAGE CURRENT**

**Saritha.M, Viji Chandran, Divya.S.Prasad, Shelja John, Sreelekshmi.J.R**

Assistant Professor, Department of EEE, College of Engineering Perumon, Kollam, Kerala, India

B.tech Scholars, Department of EEE, College of Engineering Perumon, Kollam, Kerala, India

**ABSTRACT**

Method of using transformers for providing an electrical isolation in most electrical and electronic fields are now replacing with transformerless circuits. Even though the transformers provides high efficiency, its size seems to a problem for most of the engineering works. This problem is overcome with the replacement of transformers with transformerless circuits. As a special case of consideration we are introducing a transformerless cost effective PV – grid connected system. But the presence of common leakage current (CM) between the metallic frame and the ground connection in the grid decreases the efficiency of the system. As a solution to this problem we are introducing a virtual DC bus realized with switched capacitor technology. It is found that it will reduce the leakage current to a negligible value and the problems of current ripples are avoided by ISPWM modulation techniques. The system is not only providing good efficiency but also ensuring an ecofriendly renewable energy source for future generations.

**KEYWORDS :** Photo voltaic(PV) ,Inverse sinusoidal pulse width modulation(ISPWM), Common mode leakage current(CM).

**Introduction**

The efficiency of commercial PV panels is around 15-20%. Therefore, it is very important that the power produced by these panels is not wasted, by using inefficient power electronics systems. The efficiency and reliability of both single-phase and three phase PV inverter systems can be improved using transformer less topologies. The most important advantages of transformer less PV systems are higher efficiency, smaller size and weight compared to PV systems that have galvanic isolation, but new problems related to leakage current and safety need to be dealt with. The common mode leakage current flows through the parasitic capacitance of PV panel to ground. This common mode leakage current causes system losses, reduces grid current quality, induces EMI and causes personnel safety problems.

To avoid common mode leakage current, the conventional method employs the half bridge inverter or the full bridge inverter with bipolar sinusoidal pulse width modulation to make the common mode voltage constant, which is the main cause of common

mode leakage current. But the problem is that the half inverter requires high input voltage to get the output where the full bridge inverter requires only half of the input voltage to get the same output. The main drawbacks of full bridge inverter are that it can only employ bipolar PWM with two level output, causes high current ripple and low system efficiency.

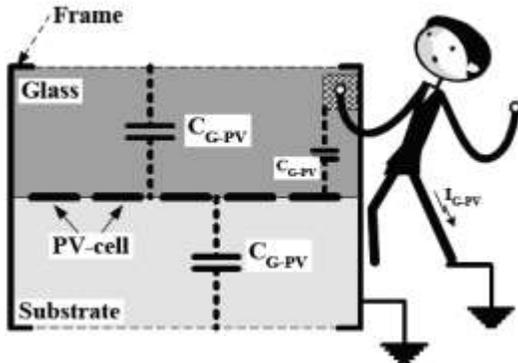
The improved transformer less topology need same low input power as the full bridge inverter and it can adopt both unipolar and double frequency PWM strategy. The main goal of this project is to analyze and model transformer less PV inverter systems with respect to the leakage current phenomenon that can damage the solar panels and pose safety problems. A new topology and modulation techniques that will minimize the leakage current and exhibits a high efficiency .

**Parasitic Capacitance Of PV Arrays**

Nowadays most photovoltaic panels have a metallic frame, which is required to be grounded in almost all countries, in order to comply with the safety regulations and standards. Since PV panels have a considerable surface area, this with the metallic

frame forms a parasitic capacitance, shown as  $C_{G-PV}$  in figure .

Figure:1



Parasitic capacitance in PV panels

The value of this parasitic capacitance depends on the:

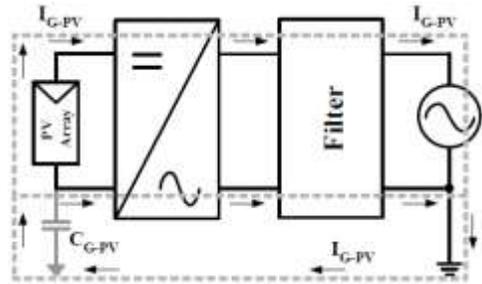
- Surface of the PV array and grounded frame
- Distance of PV cell to the module
- Atmospheric conditions
- Dust and humidity, which can increase the electrical conductivity of the panel's surface.

According to the measurements the parasitic capacitance varies between 50 nF and 150nF for each kW of installed PV panels. This parasitic capacitance is present in every PV installation and may or may not lead to leakage ground current, depending on the existence of the return path within the circuit. Since the value of this parasitic capacitance changes within wide ranges depending on construction, atmospheric conditions, etc., a value of 49 nF/kW has been chosen to be used in simulations, in order to accurately simulate the behavior of the whole PV system, with regards to the ground leakage current.

**Leakage Ground Current**

A transformerless topology lacks the galvanic isolation between the PV array and grid. This way the PV panels are directly connected to the grid, which means that there is a direct path for the leakage ground currents caused by the fluctuations of the potential between the PV array and the grid. These voltage fluctuations charge and discharge the parasitic capacitance formed between the surface of the PV and grounded frame, shown as CG-PV in Figure.

Figure:2



The path of the Alternating Ground Leakage Current

The parasitic capacitance together with the DC lines that connects the PV array to the inverter, form a resonant circuit and the resonance frequency of this circuit depends on the size of the PV array and the length of the DC cables .The path of the ground current ( $I_{G-PV}$ ) flowing through the parasitic capacitance of the PV array is shown with a grey intermittent line in Figure.2. The common-mode leakage current increases the system losses, reduces the grid-connected current quality, induces the severe conducted and radiated electromagnetic interference, and causes personal safety problems.

**Condition Of Elimination Of Leakage Current**

The ground leakage current that flows through the parasitic capacitance of the PV array is greatly influence on the common mode voltage generated by a topology. Generally the utility grid does not influence the common mode behavior of the system.The common-mode voltage can be defined as the average of the sum of voltages between the outputs and the common reference. In this case, the common reference is taken to be the negative terminal of the PV.

The differential-mode voltage is defined as the difference between the two voltages.

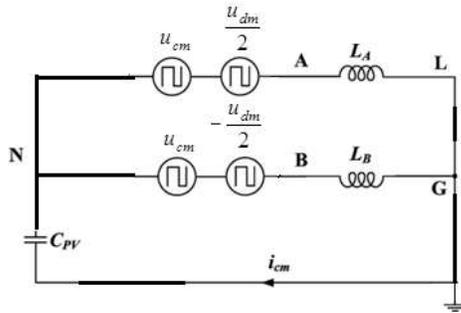
$$u_{dm} = u_{AB} = u_{AN} - u_{BN} \dots \dots \dots (2)$$

From the above two equations,

$$u_{AN} = u_{cm} + \frac{u_{dm}}{2} \dots \dots \dots (3)$$

$$u_{BN} = u_{cm} - \frac{u_{dm}}{2} \dots \dots \dots (4)$$

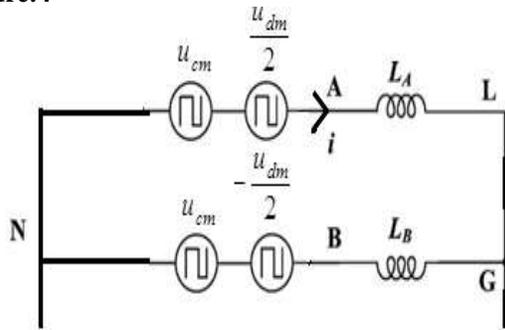
Figure:3



Model Showing the Common-Mode and Differential-Mode Voltages.

Using Thevenin's theorem in the above circuit the model can be simplified. By applying Kirchhoff's voltage law in the Fig.

Figure:4



Model to find out the Equivalent Common-Mode Voltage

To find out the current,

$$-u_{cm} - \frac{u_{dm}}{2} - iL_A - iL_B + u_{cm} - \frac{u_{dm}}{2} = 0$$

$$-u_{dm} - iL_A - iL_B = 0$$

$$-u_{dm} = iL_A + iL_B$$

$$i = -\frac{u_{dm}}{L_A + L_B} \dots \dots \dots (5)$$

To find out the  $u_{ecm}$

$$-u_{cm} - \frac{u_{dm}}{2} - iL_A + u_{ecm} = 0$$

$$u_{ecm} = u_{cm} + \frac{u_{dm}}{2} + iL_A$$

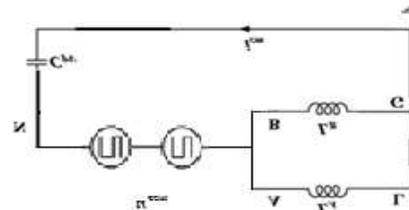
$$u_{ecm} = u_{cm} + \frac{u_{dm}}{2} + iL_A$$

$$u_{ecm} = u_{cm} + \frac{u_{dm}}{2} + L_A \left( \frac{-u_{dm}}{L_A + L_B} \right)$$

$$u_{ecm} = u_{cm} + \frac{u_{dm}}{2} \frac{L_B - L_A}{L_A + L_B} \dots \dots \dots (6)$$

The simplified equivalent model of the common-mode resonant circuit has been derived in as shown in Figure 5, where  $C_{pv}$  is the parasitic capacitor,  $L_A$  and  $L_B$  are the filter inductors,  $i_{cm}$  is the common-mode leakage current. And, an equivalent common-mode voltage  $u_{ecm}$  is defined by,

Figure:5



Simplified equivalent model of Common-mode Resonant Circuit

$$u_{ecm} = u_{cm} + \frac{u_{dm}}{2} \frac{L_B - L_A}{L_A + L_B}$$

It is clear that the common-mode leakage current  $i_{cm}$  is excited by the defined equivalent common-mode voltage  $u_{ecm}$ . Therefore, the condition of eliminating common-mode leakage current is drawn that the equivalent common-mode voltage  $u_{ecm}$  must be kept a co In the full-bridge inverter family, the filter inductors  $L_A$  and  $L_B$  are commonly selected with the same value. As a result, the condition of eliminating common-mode leakage current is met that,

$$u_{ecm} = u_{cm} + \frac{u_{dm}}{2} \frac{L_B - L_A}{L_A + L_B}$$

$$u_{ecm} = u_{cm} \frac{u_{AN} + u_{BN} + u_{CN}}{2} + \frac{u_{AN} - u_{BN} - u_{CN}}{2} \frac{L_A - L_B}{L_A + L_B} \dots (8)$$

$$= \text{constant} \dots \dots \dots (7)$$

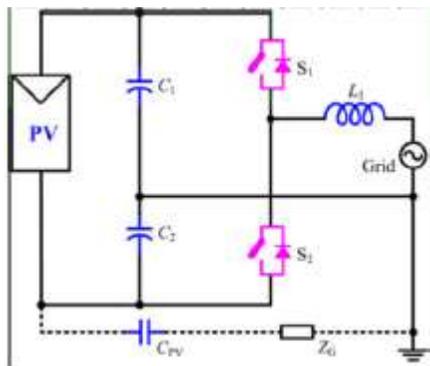
### CONVENTIONAL TOPOLOGY

Firstly, with only two switches in series, the half bridge converter is only capable of transmitting a pulse train to the output with a magnitude of half that of the full bridge. This means that for the same DC input voltage a half bridge converter may require a front end boost converter to step up the input voltage of the inverter. Introducing a new stage of the inverter will introduce charging and power devices which will result in additional losses and an overall lower efficiency.

As a higher DC input to the half bridge converter is required, it also means implemented switching device with a higher voltage rating. Such switching devices typically have higher losses and must be switched at a slower rate which may result in an increase in harmonic content of the output. It is also worth noting that the topology is only capable of implementing bipolar switching as the design consists of two switches making a freewheeling period impossible.

Another associated advantage of utilizing a half bridge topology is that the design naturally prevents DC current injection into the AC network. As a half bridge converter implements a split input capacitance, one capacitor is always present in the current conducting path.

Figure:6

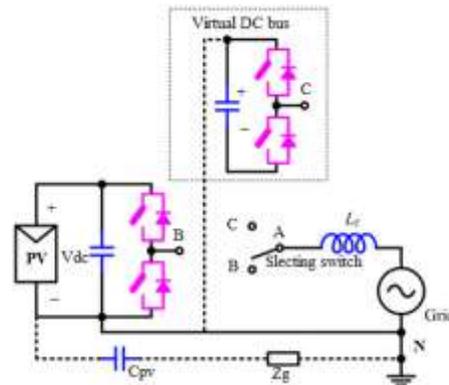


Conventional half bridge topology

**VIRTUAL DC BUS CONCEPT**

The main intention of creating a virtual DC bus is to generate a -ve output voltage necessary for the operation of inverter. A connection is made between the -ve pole of the PV panel and the grid neutral line, it will damp the voltage across the parasitic capacitor to zero. It prevents the flow of leakage current. The voltage at the midpoint B is +Vdc with respect to ground. The voltage across the virtual bus can be kept as same as the real bus, if we design it for transfer of energy between the real bus and virtual bus. The voltage at the midpoint C is zero or -Vdc.

Figure:7



Virtual DC Concept

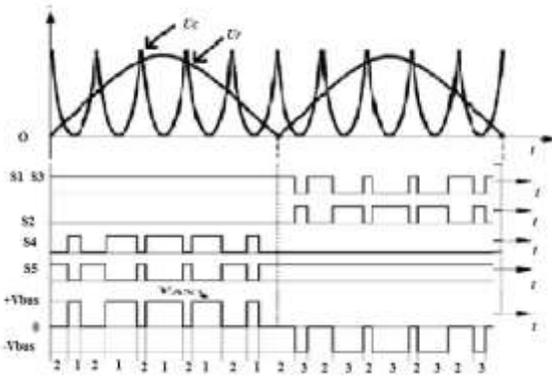
The dotted line in the figure indicates that this connection may be realized directly by a wire or indirectly by a switch. With points B and C joined together by a smart selecting switch. The voltage at point A can be of three different voltage levels namely +Vdc, zero and -Vdc. Since the CM current is eliminated naturally by the structure of the circuit, there is no limitation on the modulation strategy, which means that the advanced modulation technology such as the inverse SPWM can be used to satisfy various PV application.

**MODULATION USING ISPWM**

Modulation techniques is generally employed to reduce the current ripples. Conventional method is using PWM technique. In this method triangular wave is used as the carrier. It is evaluated that ISPWM technique gives better and higher fundamental component compared to PWM. Here inverted sine is used as a carrier and is compared with a sine wave. The pulses are generated when ever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave. The total harmonic distortion for the different values of switching frequencies is obtained and is found to be lesser than the conventional method.

By employing this new modulation technique it has been proved that the fundamental voltage is improved throughout the working range and is greater than the voltage obtained using the conventional method which employs triangular carrier for modulation.

Figure:8



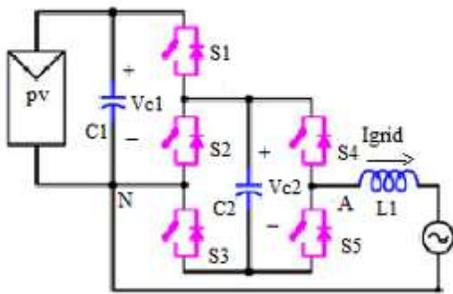
Generation of pulse using ISPWM

**PROPOSED TOPOLOGY**

Based on the -ve voltage generation concept , an inverter topology is derived to show the clear advantage of the proposed methodology.

It consist of five power switches S1- S5and only single filter inductor LF .The PV panels and capacitor C1 from the real DC bus while the virtual DC bus is provided by C2.With the switched capacitor technology,C2 is charged by the real DC bus through S1 and S3 to maintain a constant voltage.This topology can be modulated using the above discussed ISPW

Figure:9



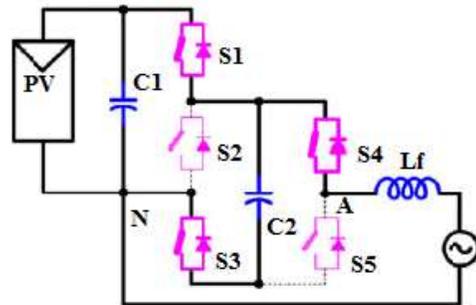
Proposed topology

**OPERATION OF PROPOSED TOPOLOGY**

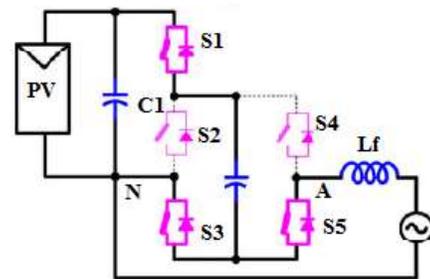
Operation of the proposed topology can be explained under 3 modes which comes alternatively after each mode.

The switches S1 S3 ON and S2 is OFF in the first mode. The commutation takes place between S4 and S5.Here S4 is ON and S5 is OFF. After the completion of this mode of operation, we get a positive output pulse of magnitude +Vbus.In the second mode of operation the switches S1, S3 ON and S2 is OFF. The commutation takes place between S4 and S5. Here S4 is OFF and S5 is ON. After the completion of this mode of operation , the output will be zero.In the third mode of operation the switches S4 is OFF and S5 is ON. The commutation is between S1S3 and S2. Here S1S3 is OFF and S2 is ON, the output will be a negative pulse. In the positive half cycle mode1 operates in between mode2. In the negative half cycle mode2 operates in between mode

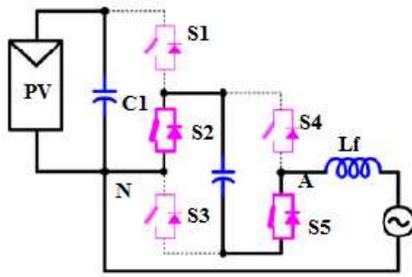
Figure:10



(a)



(b)



(c)

Operation modes (a) mode1,(b) mode2,(c) mode3

**Table:1**  
Operating Modes

MODES OF OPERATION	ON SWITCHES	OFF SWITCHES
MODE 1	S1,S3,S4	S2,S5
MODE 2	S1,S3,S5	S2,S4
MODE 3	S2,S5	S1,S4,S3

**BLOCK DIAGRAM AND HARDWARE SET UP**

The figure below shows the hardware block diagram of transformer less inverter with the virtual dc bus system. It includes

- Power Supply
- Solar Pannel
- Battery
- Mppt Solar Charge Controller
- Microcontroller Unit
- Mosfet Gate Drive Circuits
- Optocoupler Circuits

Power supply the basic unit which provides the working voltages to the microcontroller unit.it includes transformer (step down) > rectifier(AC to DC) > filters (reduces harmonics) > voltage regulators (regulate the voltage level).

A solar photovoltaic module is composed of individual PV cells of crystalline-silicon module /solar cells and has an aluminum frame and glass on the front.

Solar modules use light energy (photons) from the sun to generate electricity through the photovoltaic effect

Advantages Of Solar Panels :

- Readily available
- Long life time
- Little maintenance

Solar panels can be used as a component of a larger photovoltaic system to generate and supply electricity in commercial and residential applications. Each module is rated by its DC output power under standard test conditions (STC), and typically ranges from 100 to 320 watts. Batteries are commonly used in PV system.

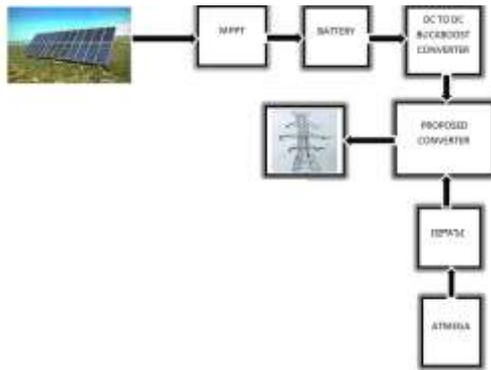
Primary functions of a storage battery are :

- Energy storage capacity and autonomy.
- Voltage and current stabilization.
- Supply surge currents.

The efficiency of a module determines the area of a module given the same rated output - an 8% efficient 230 watt module will have twice the area of a 16% efficient 230 watt module. A single solar module can produce only a limited amount of power; most installations contain multiple modules. A photovoltaic system typically includes a panel or an array of solar modules, an inverter, and sometimes a battery and/or solar tracker and interconnection wiring .Here it is connected to MPPT device.

The photovoltaic (PV) system is one of the renewable energies that attract the attention of researchers in the recent decades.The PV generators exhibit nonlinear IV and PV characteristics. The maximum power produced varies with both irradiance and temperature.Since the conversion efficiency of PV arrays is very low, it requires maximum power point tracking (MPPT) control techniques. The maximum power point tracking (MPPT) is the automatic control algorithm to adjust the power interfaces and achieve the greatest possible power harvest, during moment to moment variations of light level, shading, temperature, and photovoltaic module characteristics. The purpose of the MPPT is to adjust the solar operating voltage close to the MPP under changing atmospheric conditions.

Figure:11



Block diagram

Perturb & Observe (P&O) is the simplest method. In this we use only one sensor, that is the voltage sensor, to sense the PV array voltage and so the cost of implementation is less and hence easy to implement. The Perturb and observe algorithm states that when the operating voltage of the PV panel is perturbed by a small increment, if the resulting change in power P is positive, then we are going in the direction of MPP and we keep on perturbing in the same direction. If P is negative, we are going away from the direction of MPP and the sign of perturbation supplied has to be changed

The common mode voltage generated by the topology(proposed converter) and the modulation strategy can greatly influence the ground leakage current that flows through the parasitic capacitance of the PV array. The improved single phase transformer less topology has six switches instead of four. The additional two switches are decoupled at the dc side of the improved inverter. ISPWM pulses for these switches is given in such a way that the condition for eliminating common mode leakage current is met completely. That is the common mode voltage induced will be a constant. Simulation is done using MATLAB/SIMULINK .In order to verify the simulation results, an experimental setup has been done.The six switched improved inverter is fabricated. Generally the utility grid does not influence the common mode behavior of the system. So the generated common mode voltage of certain inverter topology and modulation strategy can be shown using a simple resistor as a load.

Figure below shows the complete hardware setup of the proposed topology

Figure:12

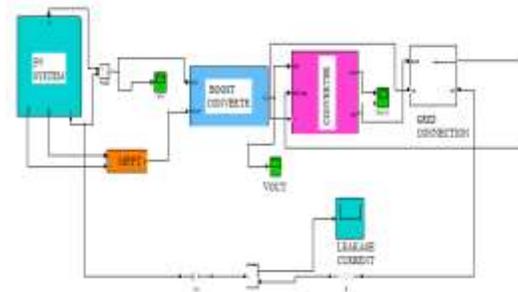


Hardware setup of the proposed topology

### SIMULINK MODEL AND EXPERIMENTAL RESULTS

Simulink model of overall system is shown below .Each blocks in the simulation diagram is designed based on the hardware components employed in the prototype .

Figure:13

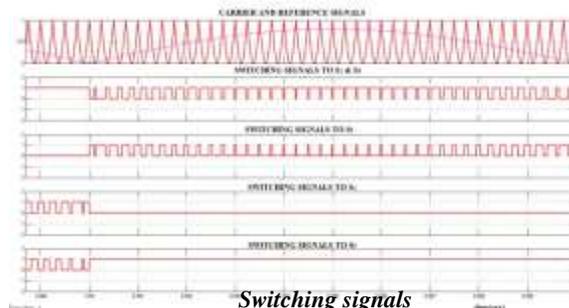


Simulink diagram

The circuit is simulated in MATLAB .Output at the each stage is verified ,mainly the output voltage of PV module , Output voltage of boost converter, Switching pulses and the leakage current.it is found that the leakage current is very much reduced to a negligible value .

### SIMULATION RESULTS

Figure:14



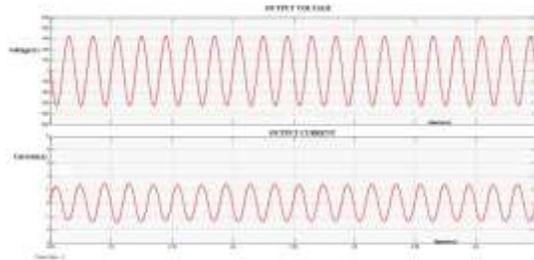
Switching signals

The switching pulses to the inverter switches are shown above. They are generated by comparing a high frequency inverse sine carrier signal with the reference sine wave.

With reference to a low power prototype the output voltage will be in a range of 20-24V and current will be in the range of 3.5-3.8A. It varies with the power rating of the PV panel employed.

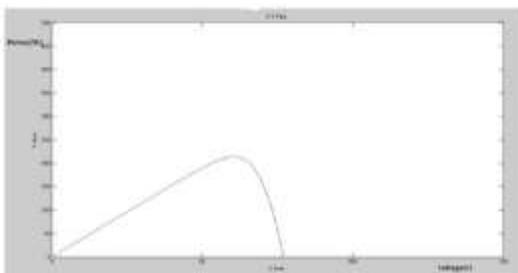
Figure below shows the leakage current while using a conventional topology. The conventional topology produces a leakage current through the parasitic capacitance between PV panel and ground. The presence of leakage current reduces grid conversion efficiency and causes various personal safety threats.

Figure:15



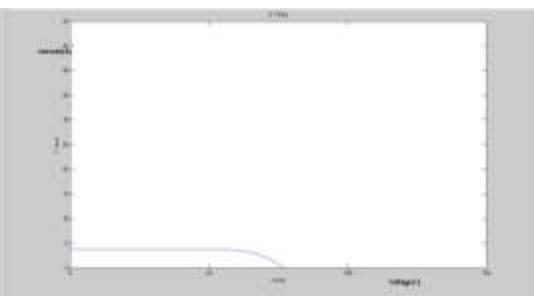
Output voltage and current waveforms

Figure:16



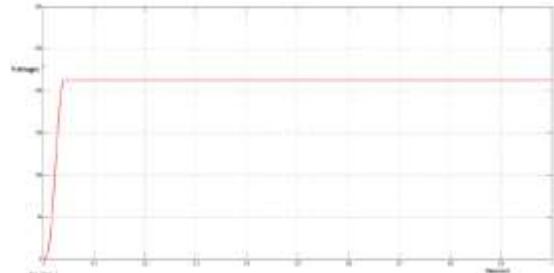
P-V output characteristics

Figure:17



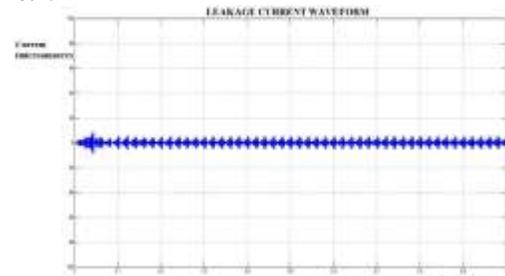
*I-V output characteristics*

Figure:18



Output Voltage Of Boost Converter

Figure:19



leakage current while using a conventional topology

Figure:20



Leakage current in the proposed topology

From the above result it is clear that in the proposed topology, the leakage current through the parasitic capacitor is zero.

**CONCLUSION AND FUTURE WORK**

The introduction of a transformerless PV-grid connected system opened a new scope of energy consumption. The concept of using a converter topology connected to virtual DC bus is put forward in this project. It can be concluded that the virtual bus concept minimized the leakage current problems, reduced the current ripples and the harmonic current distortions. By connecting the negative pole of the dc bus directly to the grid neutral

line, the voltage on the stray PV capacitor is clamped to zero. The THD of the system is analysed to check the effectiveness of the modulation strategy. The THD obtained is 4.07 % which is an acceptable range as per standards. Eliminating the CM current, using the virtual dc bus concept provides a promising solution for the transformerless grid-connected PV inverters.

## REFERENCE

- [1] E. Gubia, P. Sanchis, and A. Ursua, "Ground currents in single-phase transformerless photovoltaic systems," *Prog. Photovolt.*, vol. 15, no. 7, pp. 629–650, May 2007.
- [2] R. Ruther, A. J. G. daSilva, A. A. Montenegro, and I. T. Salamoni, "Assessment of thin-film technologies most suited for BIPV applications in Brazil: The PETROBRAS 44 kWp project," in *Proc. 3rd World Conf. Photovoltaic Energy Convers.*, Osaka, Japan, 2003, pp. 2294–2297.
- [3] X. L. Li, "Application of CIS thin film solar cells in the BIPV system with large commercial project," *New Energy Environ.*, vol. 37, pp. 46–48, 2008.
- [4] H. du Toit Mouton, "Natural balancing of three-level neutral-point clamped PWM inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1017–1025, Oct. 2002.
- [5] R. Stala, S. Pirog, M. Baszynski, A. Mondzik, A. Penczek, J. Czekonski, and S. Gasiorek, "Results of investigation of multicell converters with balancing circuit—Part I," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2610–2619, Jul. 2009.
- [6] E. Koutroulis and F. Blaabjerg, "Design optimization of grid-connected PV inverters," in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expos.*, Mar. 6–11, 2011, pp. 691–698.
- [7] T. Kerekes, R. Teodorescu, P. Rodríguez, G. Vázquez, and E. Aldabas, "A new high-efficiency single-phase transformerless PV inverter topology," *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.
- [8] O. Lopez, F. D. Freijedo, A. G. Yepes, P. Fernandez-Comesaa, J. Malvar, R. Teodorescu, and J. Doval-Gandoy, "Eliminating ground current in a transformerless photovoltaic application," *IEEE Trans. Energy Convers.*, vol. 25, no. 1, pp. 140–147, Mar. 2011.